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(bus adj1 repeater) same lock\$3	3

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L2   L1

0   L2

*DB=USPT; PLUR=YES; OP=OR*

L1   (bus adj1 repeater) same lock\$3

3   L1

END OF SEARCH HISTORY

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<u>L2</u>	L1	0	<u>L2</u>
<i>DB=USPT; PLUR=YES; OP=OR</i>			
<u>L1</u>	(bus adj1 repeater) same lock\$3	3	<u>L1</u>

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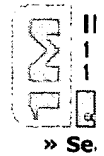
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	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
1	<input type="checkbox"/>	<input type="checkbox"/>	US 6724848 B1	20040420	8	Sync regeneration in a universal serial bus	375/368	375/211; 375/372	
2	<input type="checkbox"/>	<input type="checkbox"/>	US 6717445 B1	20040406	12	Symmetric voltage follower buffer	327/112	326/83; 327/391	
3	<input type="checkbox"/>	<input type="checkbox"/>	US 6581126 B1	20030617	28	Method, system and apparatus for a computer subsystem	710/305	370/351; 370/392;	



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bus and lock\* and (signal or pulse) and (transmit\* or

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### 1 A bus controlled clock generator IC [for TV front end]

*Kramer, R.;*

Consumer Electronics, IEEE Transactions on , Volume: 37 , Issue: 3 , Aug 19'90  
Pages:531 - 536

[\[Abstract\]](#)   [\[PDF Full-Text \(288 KB\)\]](#)   **IEEE JNL**

## 2 A single chip FSK/ASK 900 MHz transceiver in a standard 0.25 um C technology

*Schuchter, W.; Krasser, G.; Schultheiss, V.; Hofer, G.;*

Radio Frequency Integrated Circuits (RFIC) Symposium, 2001. Digest of Papers  
2001 IEEE , 20-22 May 2001  
Pages:183 - 186

[\[Abstract\]](#)   [\[PDF Full-Text \(384 KB\)\]](#)   **IEEE CNF**

### 3 Implementation of a 900 MHz transmitter system using highly integrated ASIC

*Djen, W.S.; Shah, P.M.;*

Vehicular Technology Conference, 1994 IEEE 44th , 8-10 June 1994  
Pages:1341 - 1345 vol.2

[\[Abstract\]](#) [\[PDF Full-Text \(280 KB\)\]](#) **IEEE CNF**

#### 4 A 500 Mb/s/pin quadruple data rate SDRAM interface using a skew cancellation technique

Jeongpyo Kim; Sung-Ho Wan; Joonsuk Lee; Hyoung Sik Nam; Young Gon Kim  
Hoon Shim; Hyung Ki Ahn; Seok Kang; Kyung Nam Park; Bong Hwa Jeong; J.  
Hong Ahn; Beomsup Kim;

Solid-State Circuits Conference, 2000. Digest of Technical Papers. ISSCC. 2000

IEEE International , 7-9 Feb. 2000

Pages:404 - 405

[\[Abstract\]](#) [\[PDF Full-Text \(233 KB\)\]](#) IEEE CNF

---

**5 PLL design for a 500 MB/s interface**

*Horowitz, M.; Chan, A.; Cobrunson, J.; Gasbarro, J.; Lee, T.; Leung, W.;*

*Richardson, W.; Thrush, T.; Fujii, Y.;*

Solid-State Circuits Conference, 1993. Digest of Technical Papers. 40th ISSCC

1993 IEEE International , 24-26 Feb. 1993

Pages:160 - 161, 282

[\[Abstract\]](#) [\[PDF Full-Text \(528 KB\)\]](#) IEEE CNF

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**1 IEEE P1596, a scalable coherent interface for gigabyte/sec multiprocessor applications**
*Gustavson, D.B.;*
 Nuclear Science, IEEE Transactions on , Volume: 36 , Issue: 1 , Feb. 1989  
 Pages:811 - 812

[\[Abstract\]](#)    [\[PDF Full-Text \(228 KB\)\]](#)    **IEEE JNL**
**2 Scalable coherent interface**
*Gustavson, D.B.;*
 COMPCON Spring '89. Thirty-Fourth IEEE Computer Society International Conference: Intellectual Leverage, Digest of Papers. , 27 Feb.-3 March 1989  
 Pages:536 - 538

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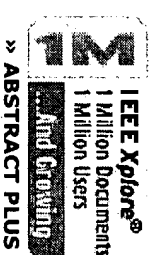
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## IEEE P1596, a scalable coherent interface for gigabyte/sec multiprocessor applications

Gustavson, D.B.

Stanford Linear Accel. Center, Stanford, CA, USA;

*This paper appears in: Nuclear Science, IEEE Transactions on*

Meeting Date: 11/09/1988 - 11/11/1988

Publication Date: Feb. 1989

Location: Orlando, FL USA

On page(s): 811 - 812

Volume: 36, Issue: 1

ISSN: 0018-9499

Reference Cited: 0

CODEN: IETNAE

Inspec Accession Number: 3420782

### Abstract:

IEEE P1596, the scalable coherent interface (SCI), formerly known as SuperBus is based on experience gained during the development of FASTBUS (IEEE 960), Futurebus (IEEE 896.1) and other modern 32-bit buses. SCI goals include a minimum bandwidth of 1 Gb/s per processor; efficient support of a coherent distributed-cache image of shared memory; and support for segmentation, **bus repeaters**, and general switched

interconnections like Banyan, Omega, or full crossbar networks. To achieve these goals, SCI must sacrifice the immediate handshake characteristics of the present generation of buses in favour of a packetlike split-cycle protocol. Wire-ORs, broadcasts, and even ordinary passive bus structures must be avoided. However, a lower performance (1 Gb/s per backplane instead of per processor) implementation using a register insertion ring architecture on a passive backplane appears to be possible using the same interface as for the more costly switch networks. The author summarizes current directions and reports the status of the work in progress

---

**Index Terms:**

[computer interfaces](#) [multiprocessing systems](#) [protocols](#) [1 Gbit/s](#) [Banyan](#) [FASTBUS](#)  
[Futurebus](#) [IEEE P1596](#) [Omega](#) [SuperBus](#) [bus repeaters](#) [coherent distributed-cache image](#)  
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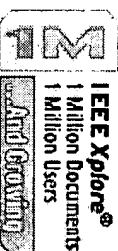
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**Scalable coherent interface**  
Gustavson, D.B.  
Stanford Linear Accel. Center, CA, USA ;  
*This paper appears in: COMPCON Spring '89. Thirty-Fourth IEEE Computer Society International Conference: Intellectual Leverage, Digest of Papers.*

Gustavson, D.B.

**Stanford Linear Accel. Center, CA, USA ;**

*This paper appears in: COMPCON Spring '89. Thirty-Fourth IEEE Computer Society*

Meeting Date: 02/27/1989 - 03/03/1989

Publication Date: 27 Feb.-3 March 1989

**Location:** San Francisco, CA USA

On page(s): 536 - 538

Reference Cited: 0

**Inspection Accession Number: 3406265**

## Abstract:

The scalable coherent interface (SCI) project (formerly known as SuperBus) is based on experience gained during the development of Fastbus (IEEE 960), Futurebus (IEEE 896.1) and other modern 32-bit buses. SCI goals include a minimum bandwidth of 1 Gb/s per processor; efficient support of a coherent distributed-cache image of shared memory; and support for segmentation, **bus repeaters**, and general switched interconnections like Banyon, Omega, or full crossbars. SCI abandons the immediate handshake characteristics of the present generation of buses in favor of a packet-based protocol. SCI avoids wire-ORs, broadcasts, and even ordinary passive bus structures,

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File: USPT

Apr 20, 2004

US-PAT-NO: 6724848

DOCUMENT-IDENTIFIER: US 6724848 B1

TITLE: Sync regeneration in a universal serial bus

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KIMC	Draw De
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☐ 2. Document ID: US 6717445 B1

L1: Entry 2 of 3

File: USPT

Apr 6, 2004

US-PAT-NO: 6717445

DOCUMENT-IDENTIFIER: US 6717445 B1

TITLE: Symmetric voltage follower buffer

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KIMC	Draw De
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☐ 3. Document ID: US 6581126 B1

L1: Entry 3 of 3

File: USPT

Jun 17, 2003

US-PAT-NO: 6581126

DOCUMENT-IDENTIFIER: US 6581126 B1

TITLE: Method, system and apparatus for a computer subsystem interconnection using a chain of bus repeaters

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KIMC	Draw De
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L3: Entry 1 of 3

File: DWPI

Apr 17, 2003

DERWENT-ACC-NO: 2003-585320

DERWENT-WEEK: 200355

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TITLE: Bus-repeater for controller area network, locks transmission of serial digital signal pulse sequence between two buses for specific time period

Basic Abstract Text (1):

NOVELTY - The bus-repeater transmits the data as serial digital signal pulse sequence between the buses (10,20). A locking unit (80) locks the transmission of pulse sequence for specific time period.

Standard Title Terms (1):

BUS REPEATER CONTROL AREA NETWORK LOCK TRANSMISSION SERIAL DIGITAL SIGNAL PULSE SEQUENCE TWO BUS SPECIFIC TIME PERIOD

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☐ 1. Document ID: US 20030074511 A1

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L3: Entry 1 of 3

File: DWPI

Apr 17, 2003

DERWENT-ACC-NO: 2003-585320

DERWENT-WEEK: 200355

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TITLE: Bus-repeater for controller area network, locks transmission of serial digital signal pulse sequence between two buses for specific time period

INVENTOR: AICHELE, A; KRAMER, J

PRIORITY-DATA: 2001US-0977466 (October 15, 2001)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
<u>US 20030074511 A1</u>	April 17, 2003		008	G06F013/38

INT-CL (IPC): G06 F 13/38

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC	Draw De
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☐ 2. Document ID: US 3110006 A

L3: Entry 2 of 3

File: USOC

Nov 5, 1963

US-PAT-NO: 3110006

DOCUMENT-IDENTIFIER: US 3110006 A

TITLE: Air traffic control system

DATE-ISSUED: November 5, 1963

INVENTOR-NAME: ALBRIGHTON REIGINALD F; SMITH WILLIS R

US-CL-CURRENT: 340/989, 340/825.28

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC	Draw De
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☐ 3. Document ID: US 2201712 A

L3: Entry 3 of 3

File: USOC

May 21, 1940

US-PAT-NO: 2201712

DOCUMENT-IDENTIFIER: US 2201712 A

TITLE: Signaling system

DATE-ISSUED: May 21, 1940

INVENTOR-NAME: BRIDGES FRANK R

US-CL-CURRENT: 340/291

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. Des
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Terms	Documents
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US006581126B1

(12) **United States Patent**  
**Regula**

(10) Patent No.: **US 6,581,126 B1**  
(45) Date of Patent: **Jun. 17, 2003**

(54) **METHOD, SYSTEM AND APPARATUS FOR A COMPUTER SUBSYSTEM INTERCONNECTION USING A CHAIN OF BUS REPEATERS**

(75) Inventor: Jack Regula, San Jose, CA (US)

(73) Assignee: PLX Technology, Inc., Sunnyvale, CA (US)

(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/315,412

(22) Filed: May 19, 1999

**Related U.S. Application Data**

(63) Continuation-in-part of application No. 08/771,581, filed on Dec. 20, 1996.

(60) Provisional application No. 60/116,686, filed on Jan. 20, 1999.

(51) Int. Cl.<sup>7</sup> ..... G06F 13/28; G06F 13/14; G06F 15/173; H04L 12/28; H04L 12/56

(52) U.S. Cl. .... 710/305; 710/31; 370/351; 370/392; 709/239; 709/242

(58) Field of Search ..... 710/305, 31, 36-38; 370/223, 351, 392-393; 713/400-601; 709/238, 239, 240, 241, 242

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A new flooding routing algorithm based on 'node-step' concept; Sheng-Lin; Jing-Sheng Lin; Singapore ICCS/ISTTA '92. 'Communications on the Move', Nov. 16-20, 1992 pp.: 1396-1399 vol. 3.\*

(List continued on next page.)

Primary Examiner—Glenn A. Aune

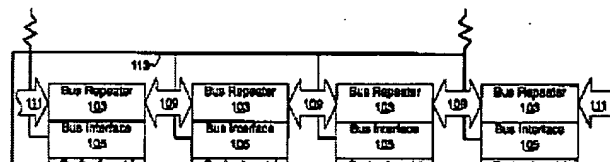
Assistant Examiner—Trisha Vu

(74) Attorney, Agent, or Firm—Swenofsky Law Group PC

(57) **ABSTRACT**

The invention discloses methods and apparatus for broadcasting information across an interconnect that includes a plurality of nodes each connected to its adjacent node(s) using one or more links. The nodes can emit cells containing transaction sub-actions onto the links. As a node receives a cell the node retransmits the cell onto other links as the cell is being received. Thus, reducing the latency imposed by the node. The node also captures the transaction sub-action while it the cell is retransmitted. The node responds to the transaction sub-action by manipulating shared handshake lines that are bussed with the other nodes. The invention enables snooping cache protocols to be successfully used in a larger multi-processor computer system than the prior art.

69 Claims, 12 Drawing Sheets



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File: USPT

Sep 15, 1998

US-PAT-NO: 5809077

DOCUMENT-IDENTIFIER: US 5809077 A

TITLE: Circuit for signal-transmitting connection of data networks

DATE-ISSUED: September 15, 1998

INT-CL: [06] H04 B 10/24

US-CL-ISSUED: 375/257; 370/287, 359/111, 359/113, 359/161, 359/173, 178/73, 379/407

US-CL-CURRENT: 375/257; 178/73, 370/287, 379/406.04

FIELD-OF-SEARCH: 375/211, 375/213, 375/214, 375/219, 375/220, 375/224, 375/257,  
375/258, 375/377, 370/241, 370/248, 370/276, 370/282, 370/286, 370/287, 370/296,  
379/344, 379/406, 379/407, 379/410, 379/414, 379/416, 178/71.1, 178/73, 364/DIG.1,  
364/DIG.2, 359/111, 359/113, 359/152, 359/161, 359/173

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L3: Entry 1 of 1

File: USPT

Mar 26, 2002

US-PAT-NO: 6363066

DOCUMENT-IDENTIFIER: US 6363066 B1

TITLE: Method and arrangement for combined data and power distribution using a communication bus

DATE-ISSUED: March 26, 2002

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Frimodig; Hans-Ove	Goteborg			SE

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Mecel AB				SE	03

APPL-NO: 09/ 155389   [\[PALM\]](#)

DATE FILED: September 28, 1998

## FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
SE	9700633	February 21, 1997

## PCT-DATA:

APPL-NO	DATE-FILED	PUB-NO	PUB-DATE	371-DATE	102(E)-DATE
PCT/SE98/00267	February 13, 1998	WO98/37642	Aug 27, 1998	Sep 28, 1998	Sep 28, 1998

INT-CL: [07] [H04](#) [L](#) [12/50](#)

US-CL-ISSUED: 370/360; 370/489, 710/110

US-CL-CURRENT: [370/360](#); [370/489](#), [710/110](#)

FIELD-OF-SEARCH: 370/464, 370/465, 370/489, 370/490, 370/360, 370/248, 370/282, 370/400, 370/437, 370/438, 370/439, 370/451, 714/100, 714/2, 714/4, 375/257, 710/100, 710/107, 710/110

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

**Search Selected****Search ALL****Clear**

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<u>5321689</u>	June 1994	Suzuki	370/228
<input type="checkbox"/>	<u>5446846</u>	August 1995	Lennartsson	710/100
<input type="checkbox"/>	<u>5572658</u>	November 1996	Mohr	714/4
<input type="checkbox"/>	<u>5592485</u>	January 1997	Consiglieri	370/360
<input type="checkbox"/>	<u>5617282</u>	April 1997	Rall	361/56
<input type="checkbox"/>	<u>5809077</u>	September 1998	Dorner	375/257

## FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
4438836	April 1995	DE	
19501887	July 1995	DE	
4425250	January 1996	DE	
19520596	December 1996	DE	
0656696	June 1995	EP	
9604735	February 1996	WO	

ART-UNIT: 2661

PRIMARY-EXAMINER: Olms; Douglas

ASSISTANT-EXAMINER: Pizarro; Ricardo M.

ATTY-AGENT-FIRM: Ostrolenk, Faber, Gerb &amp; Soffen, LLP

## ABSTRACT:

A method and arrangement for combined data- and power distribution between nodes (MA, SL, SL.sub.N) in distributed data processing systems having a common communication bus (1, CAN.sub.H /CAN.sub.L) in which the communication bus includes at least one wire or differentiated dual wires transmitting digital information serially in form of dominant data bits at a first signal level (U.sub.1 /U.sub.3 V/.sub.D2) and recessive data bits at a second lower signal level (U.sub.2, V.sub.D1) in a sequential order dependent on the content of the data being transmitted. Nodes (SL) having a low power consumption obtain power supply through dominant bits being transmitted on the bus (1), which dominant bits charge a capacitance (15) in the low effect nodes (SL). Nodes (MA) having a higher power consumption obtain power supply from a voltage source (V.sub.1) separated from the bus. At least one node (MA) of the high effect nodes includes an amplification unit (20-24) which will be activated automatically in order to amplify the potential of dominant bits being transmitted by a low effect node.

12 Claims, 4 Drawing figures

# Hit List

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## Search Results - Record(s) 1 through 3 of 3 returned.

☐ 1. Document ID: US 3912884 A

L4: Entry 1 of 3

File: USPT

Oct 14, 1975

US-PAT-NO: 3912884

DOCUMENT-IDENTIFIER: US 3912884 A

TITLE: Communication monitoring system

DATE-ISSUED: October 14, 1975

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Membrino; Robert J.	Silver Spring	MD		
Ridgell, Jr.; James J.	Elkridge	MD		

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
The Singer Company	New York	NY			02

APPL-NO: 05/ 494389 [PALM]

DATE FILED: August 5, 1974

INT-CL: [02] H04B 3/46

US-CL-ISSUED: 179/175.3R; 179/175.2C

US-CL-CURRENT: 370/241

FIELD-OF-SEARCH: 179/175.2C, 179/175.3R, 179/175.31R, 179/170.2, 333/10

PRIOR-ART-DISCLOSED:

## U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<u>3560669</u>	February 1971	Foulkes et al.	179/170.2
<u>3637955</u>	January 1972	Tilly et al.	179/175.31R
<u>3823275</u>	July 1974	La Marche et al.	179/170.2

ART-UNIT: 232

h e b b cg b e e ch

PRIMARY-EXAMINER: Olms; Douglas W.

ATTY-AGENT-FIRM: Grobman; William Kesterson; James C.

ABSTRACT:

The invention of this disclosure comprises a system for monitoring the flow of information along a single transmission path where the information may be transmitted from both directions. The apparatus of this invention comprises means for receiving information moving along the transmission path in either direction, means for delaying that information, a first directional path and a second directional path, means for inhibiting the flow along one of said paths by the receipt of information moving along the other path, and means for monitoring the information along the two paths by any suitable means.

9 Claims, 2 Drawing figures

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw D
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☐ 2. Document ID: US 3832489 A

L4: Entry 2 of 3

File: USPT

Aug 27, 1974

US-PAT-NO: 3832489

DOCUMENT-IDENTIFIER: US 3832489 A

TITLE: BIDIRECTIONAL BUS REPEATER

DATE-ISSUED: August 27, 1974

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Krishna; Rallapalli	Maynard	MA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Digital Equipment Corporation	Maynard	MA			02

APPL-NO: 05/ 334951 [PALM]

DATE FILED: February 26, 1973

INT-CL: [] H041 25/20

US-CL-ISSUED: 178/71R

US-CL-CURRENT: 178/71.1

FIELD-OF-SEARCH: 179/17R, 179/17NC, 178/7R, 178/71R

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<u>3612781</u>	October 1971	Da Costa et al.	179/170NC
<u>3673326</u>	June 1972	Lee	178/71R

ART-UNIT: 233

PRIMARY-EXAMINER: Claffy; Kathleen H.

ASSISTANT-EXAMINER: Saffian; Mitchell

ATTY-AGENT-FIRM: Cesari and McKenna

## ABSTRACT:

A bus repeater circuit for interconnecting first and second corresponding transmission lines for first and second adjacent bidirectional electrical bus sections. The bus repeater circuit includes first and second current sensors associated with each transmission line to apply a bipolar signal to first and second amplifiers respectively. Output signals from a given sensor of a first polarity indicate that the associated transmission line is transmitting a signal. The associated amplifier couples that signal to the other bus wire. Signals of a second polarity indicate that the associated bus transmission line is not transmitting a signal to the repeater and the associated amplifier provides a corresponding signal, thereby avoiding a latched condition.

6 Claims, 1 Drawing figures

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMIC	Draw. De
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☐ 3. Document ID: US 3673326 A

L4: Entry 3 of 3

File: USPT

Jun 27, 1972

US-PAT-NO: 3673326

DOCUMENT-IDENTIFIER: US 3673326 A

**\*\* See image for Certificate of Correction \*\***

TITLE: COMMUNICATION SYSTEM

DATE-ISSUED: June 27, 1972

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Lee; Francis F.	Lexington	MA	02173	

APPL-NO: 05/ 064374 [PALM]

DATE FILED: August 17, 1970

INT-CL: [] H041 25/40

US-CL-ISSUED: 178/71R

US-CL-CURRENT: 178/71.1

h e b b c g b e e ch



FIELD-OF-SEARCH: 178/71R, 178/7R

PRIOR-ART-DISCLOSED:

## U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<u>3410957</u>	November 1968	Schiebeler	178/71R
<u>3499985</u>	March 1970	Rowlands	178/70R

ART-UNIT: 232

PRIMARY-EXAMINER: Claffy; Kathleen H.

ASSISTANT-EXAMINER: Helvestine; William A.

ATTY-AGENT-FIRM: Ertman; Willis M.

## ABSTRACT:

A bilateral repeater for connection in a transmission line arranged to transmit data between two spaced points includes a network having two inputs and two outputs. Each output is connected to a corresponding input at a terminal arranged for connection to the transmission line. The repeater also includes bilateral circuitry responsive to an initiating data signal applied via either of the terminals to an input for transmitting a corresponding data signal via an output to the other of the terminals only as long as the initiating data signal continues to be applied at the first terminal, and the bilateral circuitry includes an inhibiting circuit for preventing transmission of corresponding data signals if initiating data signals are applied at both of the terminals at the same time.

21 Claims, 4 Drawing figures

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KIMC	Draw. De
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L11: Entry 1 of 4

File: USPT

Sep 10, 2002

US-PAT-NO: 6448810

DOCUMENT-IDENTIFIER: US 6448810 B1

TITLE: Bidirectional bus-repeater controller

DATE-ISSUED: September 10, 2002

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Nomura; Masahiro	Tokyo			JP

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
NEC Corporation	Tokyo			JP	03

APPL-NO: 09/ 482513   [PALM]

DATE FILED: January 14, 2000

## FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	11-007678	January 14, 1999

INT-CL: [07] H03 K 19/017

US-CL-ISSUED: 326/82; 326/112

US-CL-CURRENT: 326/82; 326/112

FIELD-OF-SEARCH: 326/82, 326/83, 326/86, 326/56-58, 326/112, 326/119

PRIOR-ART-DISCLOSED:

## U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<u>5214330</u>	May 1993	Okazaki	326/90
<input type="checkbox"/>	<u>5248908</u>	September 1993	Kimura	326/38
<input type="checkbox"/>	<u>5274769</u>	December 1993	Ishida	710/31
<input type="checkbox"/>	<u>5726589</u>	March 1998	Cahill et al.	326/81
<input type="checkbox"/>	<u>5736870</u>	April 1998	Greason et al.	326/80

## FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
57-187726	November 1982	JP	326/58
2-211567	August 1990	JP	
03007424	January 1991	JP	

## OTHER PUBLICATIONS

Rhyne, "Fundamental of Digital Systems Design", N.J., 1973, pp. 70-71, 1973.

ART-UNIT: 2819

PRIMARY-EXAMINER: Tokar; Michael

ASSISTANT-EXAMINER: Cho; James H.

ATTY-AGENT-FIRM: Sughrue Mion, PLLC

## ABSTRACT:

The present invention provides a bidirectional bus repeater controller comprising: a bidirectional bus line for bidirectional transmissions of signals; at least a bidirectional repeater on the bidirectional bus line for controlling bidirectional transmissions of signals on the bidirectional bus line; at least a bus driver connected to the bidirectional bus line for transmitting inputted signals to the bidirectional bus line in accordance with a bus driver control signal; at least a bus receiver connected to the bidirectional bus line for receiving signals from the bidirectional bus line; and a logic circuit extending along the bidirectional bus line and being connected to the at least bidirectional repeater for transmitting bidirectional bus repeater control signals to the at least bidirectional repeater upon input of the bus driver control signal.

24 Claims, 27 Drawing figures

First Hit   Fwd Refs

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L11: Entry 3 of 4

File: USPT

Apr 23, 2002

US-PAT-NO: 6378084

DOCUMENT-IDENTIFIER: US 6378084 B1

TITLE: Enclosure processor with failover capability

DATE-ISSUED: April 23, 2002

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Strunk; Glenn W.	Ft. Collins	CO		
Erickson; Michael J.	Loveland	CO		
Zilavy; Daniel V.	Ft. Collins	CO		

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hewlett-Packard Company	Palo Alto	CA			02

APPL-NO: 09/ 277219   [PALM]

DATE FILED: March 29, 1999

INT-CL: [07] G06 F 11/00

US-CL-ISSUED: 714/2; 711/112

US-CL-CURRENT: 714/2; 711/112

FIELD-OF-SEARCH: 714/2, 714/4, 714/5, 714/6, 714/7, 714/8, 714/10-12, 714/25, 714/31, 714/39, 714/42, 714/43, 711/112, 711/114, 709/201, 709/203

PRIOR-ART-DISCLOSED:

## U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<u>4509113</u>	April 1985	Heath	
<input type="checkbox"/>	<u>4710926</u>	December 1987	Brown et al.	714/4
<input type="checkbox"/>	<u>5337414</u>	August 1994	Hashemi et al.	710/52
<input type="checkbox"/>	<u>5471586</u>	November 1995	Sefidvash et al.	710/104
<input type="checkbox"/>	<u>5560033</u>	September 1996	Doherty et al.	713/340
<input type="checkbox"/>	<u>5586250</u>	December 1996	Carbonneau et al.	395/183.2

<input type="checkbox"/>	<u>5781798</u>	July 1998	Beatty et al.	710/10
<input type="checkbox"/>	<u>5864689</u>	January 1999	Tran	712/208
<input type="checkbox"/>	<u>5901298</u>	May 1999	Cummins et al.	711/5
<input type="checkbox"/>	<u>5974491</u>	October 1999	Jung et al.	710/106
<input type="checkbox"/>	<u>6038680</u>	March 2000	Olarig	714/6
<input type="checkbox"/>	<u>6061806</u>	May 2000	Caldwell et al.	714/3
<input type="checkbox"/>	<u>6173374</u>	January 2001	Heil et al.	711/148
<input type="checkbox"/>	<u>6253334</u>	June 2001	Amdahl et al.	714/4

ART-UNIT: 2184

PRIMARY-EXAMINER: Iqbal; Nadeem

ABSTRACT:

A device and method for enclosure processing of a dual SCSI bus enclosure is described. A single SCSI enclosure processor is provided on an adapter that can operate alone or in pairs to provide different modes of operation, including simplex, duplex, and cluster. When used in pairs, two adapters interconnect internally to the enclosure through internal cross-coupling bus repeaters. The adapters have the ability to automatically configure themselves. In the cluster mode, a first enclosure processor on a first adapter assumes an active status, while a second enclosure processor on a second adapter waits in a standby mode. The standby enclosure processor detects when the active enclosure processor has failed, misoperated, or been removed and automatically failover, assuming the identity of the active enclosure processor, without disruption to the system. Hot-swapping of the adapter boards is therefore possible.

18 Claims, 9 Drawing figures

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L11: Entry 3 of 4

File: USPT

Apr 23, 2002

US-PAT-NO: 6378084

DOCUMENT-IDENTIFIER: US 6378084 B1

TITLE: Enclosure processor with failover capability

DATE-ISSUED: April 23, 2002

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Strunk; Glenn W.	Ft. Collins	CO		
Erickson; Michael J.	Loveland	CO		
Zilavy; Daniel V.	Ft. Collins	CO		

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hewlett-Packard Company	Palo Alto	CA			02

APPL-NO: 09/ 277219   [PALM]

DATE FILED: March 29, 1999

INT-CL: [07] G06 F 11/00

US-CL-ISSUED: 714/2; 711/112

US-CL-CURRENT: 714/2; 711/112

FIELD-OF-SEARCH: 714/2, 714/4, 714/5, 714/6, 714/7, 714/8, 714/10-12, 714/25, 714/31, 714/39, 714/42, 714/43, 711/112, 711/114, 709/201, 709/203

PRIOR-ART-DISCLOSED:

## U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<u>4509113</u>	April 1985	Heath	
<input type="checkbox"/>	<u>4710926</u>	December 1987	Brown et al.	714/4
<input type="checkbox"/>	<u>5337414</u>	August 1994	Hashemi et al.	710/52
<input type="checkbox"/>	<u>5471586</u>	November 1995	Sefidvash et al.	710/104
<input type="checkbox"/>	<u>5560033</u>	September 1996	Doherty et al.	713/340
<input type="checkbox"/>	<u>5586250</u>	December 1996	Carbonneau et al.	395/183.2

<input type="checkbox"/>	<u>5781798</u>	July 1998	Beatty et al.	710/10
<input type="checkbox"/>	<u>5864689</u>	January 1999	Tran	712/208
<input type="checkbox"/>	<u>5901298</u>	May 1999	Cummins et al.	711/5
<input type="checkbox"/>	<u>5974491</u>	October 1999	Jung et al.	710/106
<input type="checkbox"/>	<u>6038680</u>	March 2000	Olarig	714/6
<input type="checkbox"/>	<u>6061806</u>	May 2000	Caldwell et al.	714/3
<input type="checkbox"/>	<u>6173374</u>	January 2001	Heil et al.	711/148
<input type="checkbox"/>	<u>6253334</u>	June 2001	Amdahl et al.	714/4

ART-UNIT: 2184

PRIMARY-EXAMINER: Iqbal; Nadeem

ABSTRACT:

A device and method for enclosure processing of a dual SCSI bus enclosure is described. A single SCSI enclosure processor is provided on an adapter that can operate alone or in pairs to provide different modes of operation, including simplex, duplex, and cluster. When used in pairs, two adapters interconnect internally to the enclosure through internal cross-coupling bus repeaters. The adapters have the ability to automatically configure themselves. In the cluster mode, a first enclosure processor on a first adapter assumes an active status, while a second enclosure processor on a second adapter waits in a standby mode. The standby enclosure processor detects when the active enclosure processor has failed, misoperated, or been removed and automatically failover, assuming the identity of the active enclosure processor, without disruption to the system. Hot-swapping of the adapter boards is therefore possible.

18 Claims, 9 Drawing figures

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L11: Entry 4 of 4

File: USPT

Feb 16, 1993

US-PAT-NO: 5187660

DOCUMENT-IDENTIFIER: US 5187660 A

TITLE: Arrangement for displaying on a display volumetric data

DATE-ISSUED: February 16, 1993

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Civanlar; M. Reha	Red Bank	NJ		
Dzik; Steven C.	Somerset	NJ		
Liow; Yuh-Tay	Edison	NJ		

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
AT&T Bell Laboratories	Murray Hill	NJ			02

APPL-NO: 07/ 444227   [PALM]

DATE FILED: December 1, 1989

INT-CL: [05] G06F 15/00

US-CL-ISSUED: 364/413.19; 395/119, 395/124

US-CL-CURRENT: 345/424; 345/419

FIELD-OF-SEARCH: 364/413.19, 395/124, 395/120, 395/119, 340/729

PRIOR-ART-DISCLOSED:

## U.S. PATENT DOCUMENTS

**Search Selected****Search ALL****Clear**

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<u>4539639</u>	September 1985	LeCog et al.	364/414
<input type="checkbox"/>	<u>4719585</u>	January 1988	Cline et al.	395/124
<input type="checkbox"/>	<u>4827413</u>	May 1989	Baldwin et al.	364/413.19
<input type="checkbox"/>	<u>5068808</u>	November 1991	Wake	395/119

## OTHER PUBLICATIONS



Patent application, "High Resolution Graphics Machine Architecture", Howard-McMillan-Potmesil 1-1-1.

"The Pixel Machine System Architecture", AT&T-Pixel Machines, Crawfords Corner Rd., Holmdel, N.J. 07733.

IEEE Computer Graphics and Applications, Jan. 1985, "Back-to-Front Display of Voxel-Based Objects", G. Frieder, et al, pp. 52-59.

Computer Graphics, vol. 22, No. 4, Aug. 1988, "Volume Rendering", R. A. Drebin et al, pp. 65-74.

ART-UNIT: 231

PRIMARY-EXAMINER: Envall, Jr.; Roy N.

ASSISTANT-EXAMINER: Bai; Ari

ATTY-AGENT-FIRM: Luludis; F. B.

ABSTRACT:

A facility is provided for greatly enhancing the rate at which volumetric data is processed by display on a two-dimensional display. Specifically, the volumetric data is first divided into a predetermined number of sub-blocks, in which a predetermined voxel in each sub-block is then transformed into an associated picture element. The sub-blocks and their associated pixels are then supplied to respective processors forming an array of processors. Each processor then completes the transformation of its sub-block as a function of the coordinates of the associated picture element and respective incremental vectors.

10 Claims, 9 Drawing figures

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L16: Entry 1 of 29

File: USPT

Apr 20, 2004

US-PAT-NO: 6724848

DOCUMENT-IDENTIFIER: US 6724848 B1

TITLE: Sync regeneration in a universal serial bus

DATE-ISSUED: April 20, 2004

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Iyer; Venkat	Beaverton	OR		

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Intel Corporation	Santa Clara	CA			02

APPL-NO: 09/ 519511    [PALM]

DATE FILED: March 6, 2000

INT-CL: [07] H04 L 7/00

US-CL-ISSUED: 375/368; 375/211, 375/372

US-CL-CURRENT: 375/368; 375/211, 375/372

FIELD-OF-SEARCH: 375/211, 375/213, 375/373, 375/374, 375/214, 375/215, 375/372, 375/362, 375/365, 375/366, 375/368, 710/300, 710/108, 710/305, 710/310, 370/503, 370/509

PRIOR-ART-DISCLOSED:

## U.S. PATENT DOCUMENTS

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PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/> <u>5457718</u>	October 1995	Anderson et al.	375/373
<input type="checkbox"/> <u>5963602</u>	October 1999	Aoki et al.	375/354
<input type="checkbox"/> <u>6111437</u>	August 2000	Patel	327/74
<input type="checkbox"/> <u>6298103</u>	October 2001	Huang et al.	375/355
<input type="checkbox"/> <u>6381666</u>	April 2002	Kejser et al.	710/300
<input type="checkbox"/> <u>6487155</u>	November 2002	Carson et al.	369/59.13
<input type="checkbox"/> <u>6536011</u>	March 2003	Jang et al.	714/814

☐ 2002/0176526

November 2002

Mejia

375/372

ART-UNIT: 2631

PRIMARY-EXAMINER: Corrielus; Jean B.

ATTY-AGENT-FIRM: Yates; Steven D.

## ABSTRACT:

A Universal Serial Bus repeater is provided, comprising a method and apparatus for detecting a specified data pattern and regenerating or retransmitting the recognized data pattern. In some embodiments, the invention recognizes an end of sync signal, and is operable to retransmit the end of sync signal and the following data that is presumed to be valid as a result of sync recognition. In other embodiments, the invention recognizes and retransmits a properly aligned end of packet signal, the size of which is dependent on detection of whether the end of packet signal is a part of a start of frame packet.

10 Claims, 3 Drawing figures

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L16: Entry 3 of 29

File: USPT

Jan 6, 2004

US-PAT-NO: 6675244

DOCUMENT-IDENTIFIER: US 6675244 B1

TITLE: SCSI data rate speed determination

DATE-ISSUED: January 6, 2004

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Elliott; Robert C.	Houston	TX		
Galloway; William C.	Houston	TX		

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE	CODE
Hewlett-Packard Development Company, L.P.	Fort Collins	CO			02	

APPL-NO: 09/ 507000   [\[PALM\]](#)

DATE FILED: February 18, 2000

## PARENT-CASE:

This application claims the benefit of U.S. Provisional Application No. 60/120,838, filed Feb. 19, 1999, which is incorporated herein by reference.

INT-CL: [07] [G06](#) [F](#) [13/16](#)

US-CL-ISSUED: 710/107; 710/33, 710/60, 710/107

US-CL-CURRENT: [710/107](#); [710/33](#), [710/60](#)

FIELD-OF-SEARCH: 710/33, 710/60, 710/107

PRIOR-ART-DISCLOSED:

## U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<a href="#">5450548</a>	September 1995	Matsushima	710/61
<input type="checkbox"/>	<a href="#">5463743</a>	October 1995	Galloway	395/285
<input type="checkbox"/>	<a href="#">5522054</a>	May 1996	Gunlock et al.	395/439
<input type="checkbox"/>	<a href="#">5613074</a>	March 1997	Galloway	395/280

<input type="checkbox"/>	<u>5675723</u>	October 1997	Ekrot et al.	395/182.02
<input type="checkbox"/>	<u>5692200</u>	November 1997	Carlson et al.	395/735
<input type="checkbox"/>	<u>5751977</u>	May 1998	Alexander	395/306
<input type="checkbox"/>	<u>5878039</u>	March 1999	Gorshe et al.	370/376
<input type="checkbox"/>	<u>5925120</u>	July 1999	Arp et al.	710/131
<input type="checkbox"/>	<u>5930483</u>	July 1999	Cummings et al.	710/107
<input type="checkbox"/>	<u>6012105</u>	January 2000	Rubbmark et al.	710/14
<input type="checkbox"/>	<u>6140850</u>	October 2000	Inoue	327/141
<input type="checkbox"/>	<u>6223244</u>	April 2001	Downer et al.	710/244

ART-UNIT: 2182

PRIMARY-EXAMINER: Gaffin; Jeffrey

ASSISTANT-EXAMINER: Farooq; Mohammad O.

ABSTRACT:

The method of the present invention enables a SCSI repeater to dynamically determine the speed of an input device and adjust the repeater's output speed accordingly. Thus, the SCSI repeater can transparently connect independent SCSI buses that are connected to different devices with different requirements, preventing the slowest device from limiting the speed of the fastest device.

34 Claims, 15 Drawing figures

First Hit   Fwd Refs☐  

L16: Entry 4 of 29

File: USPT

Oct 21, 2003

US-PAT-NO: 6636921

DOCUMENT-IDENTIFIER: US 6636921 B1

TITLE: SCSI repeater circuit with SCSI address translation and enable

DATE-ISSUED: October 21, 2003

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Scholhamer; George J.	Tomball	TX		
Galloway; William C.	Houston	TX		

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hewlett-Packard Development Company, LP.	Houston	TX			02

APPL-NO: 09/ 507278   [PALM]

DATE FILED: February 18, 2000

## PARENT-CASE:

SPECIFICATION This application claims the benefit of U.S. Provisional Application No. 60/120,938, filed Feb. 19, 1999, which is incorporated herein by reference.

INT-CL: [07] G06 F 13/00

US-CL-ISSUED: 710/305; 710/314, 710/315, 714/2, 714/4

US-CL-CURRENT: 710/305; 710/314, 710/315, 714/2, 714/4

FIELD-OF-SEARCH: 710/305, 710/314, 710/315, 710/110, 710/2, 710/312, 714/2, 714/4

PRIOR-ART-DISCLOSED:

## U.S. PATENT DOCUMENTS

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<u>5239632</u>	August 1993	Larner	710/314
<input type="checkbox"/>	<u>5463743</u>	October 1995	Galloway	395/285
<input type="checkbox"/>	<u>5522054</u>	May 1996	Gunlock et al.	395/439
<input type="checkbox"/>	<u>5613074</u>	March 1997	Galloway	395/280
<input type="checkbox"/>	<u>5675723</u>	October 1997	Ekrot et al.	395/182.02

<input type="checkbox"/>	<u>5692200</u>	November 1997	Carlson et al.	395/735
<input type="checkbox"/>	<u>5740386</u>	April 1998	Miller et al.	710/306
<input type="checkbox"/>	<u>5751977</u>	May 1998	Alexander	395/306
<input type="checkbox"/>	<u>5771359</u>	June 1998	Galloway et al.	710/310
<input type="checkbox"/>	<u>5925120</u>	July 1999	Arp et al.	710/300
<input type="checkbox"/>	<u>5970236</u>	October 1999	Galloway et al.	712/300
<input type="checkbox"/>	<u>6408343</u>	June 2002	Erickson et al.	710/15

ART-UNIT: 2181

PRIMARY-EXAMINER: Dharia; Rupal

ABSTRACT:

The present invention relates to a repeater circuit for providing effective point-to-point coupling between terminated Small Computer System Interface (SCSI) bus segments. The repeater circuit has an enable input and can perform SCSI address translation to map SCSI addresses from a narrow SCSI bus to high SCSI addresses on a wide SCSI bus.

19 Claims, 12 Drawing figures

First Hit   Fwd Refs☐  

L16: Entry 5 of 29

File: USPT

Apr 29, 2003

US-PAT-NO: 6557064

DOCUMENT-IDENTIFIER: US 6557064 B1

TITLE: Set up time adjust

DATE-ISSUED: April 29, 2003

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Galloway; William C.	Houston	TX		

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE	CODE
Hewlett-Packard Development Company	Palo Alto	CA				02

APPL-NO: 09/ 507071   [PALM]

DATE FILED: February 18, 2000

## PARENT-CASE:

SPECIFICATION This application claims the benefit of U.S. Provisional Application No. 60/120,980, filed Feb. 19, 1999, which is incorporated herein by reference.

INT-CL: [07] G06 F 13/24

US-CL-ISSUED: 710/260

US-CL-CURRENT: 710/260

FIELD-OF-SEARCH: 710/107, 710/312, 710/260

PRIOR-ART-DISCLOSED:

## U.S. PATENT DOCUMENTS

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<u>5463743</u>	October 1995	Galloway	395/285
<input type="checkbox"/>	<u>5522054</u>	May 1996	Gunlock et al.	395/439
<input type="checkbox"/>	<u>5613074</u>	March 1997	Galloway	395/280
<input type="checkbox"/>	<u>5675723</u>	October 1997	Ekrot et al.	395/182.02
<input type="checkbox"/>	<u>5692200</u>	November 1997	Carlson et al.	395/735
<input type="checkbox"/>	<u>5751977</u>	May 1998	Alexander	395/306



<input type="checkbox"/> <u>6078979</u>	June 2000	Li et al.	710/312
<input type="checkbox"/> <u>6317417</u>	November 2001	Childs et al.	710/107

ART-UNIT: 2181

PRIMARY-EXAMINER: Auve; Glenn A.

ASSISTANT-EXAMINER: Glass; David

ATTY-AGENT-FIRM: Akin Gump Strauss Hauer & Feld LLP

ABSTRACT:

The present invention relates generally to a method for improving the throughput of data transfers on a bus. More specifically, data setup and hold times relative to REQ# and ACK# signal edges are adjusted programmatically to provide greater integrity in the transmission of data.

21 Claims, 9 Drawing figures

First Hit   Fwd Refs

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L16: Entry 7 of 29

File: USPT

Dec 10, 2002

US-PAT-NO: 6493785

DOCUMENT-IDENTIFIER: US 6493785 B1

TITLE: Communication mode between SCSI devices

DATE-ISSUED: December 10, 2002

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Galloway; William C.	Houston	TX		

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE	CODE
Compaq Information Technologies Group, L.P.	Houston	TX				02

APPL-NO: 09/ 506709   [PALM]

DATE FILED: February 18, 2000

## PARENT-CASE:

SPECIFICATION This application claims the benefit of U.S. Provisional Application No. 60/120,839, filed Feb. 19, 1999, which is incorporated herein by reference.

INT-CL: [07] G06 F 13/36

US-CL-ISSUED: 710/314; 710/313, 710/105

US-CL-CURRENT: 710/314; 710/105, 710/313

FIELD-OF-SEARCH: 710/314, 710/313, 710/105

PRIOR-ART-DISCLOSED:

## U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<u>5463743</u>	October 1995	Galloway	395/285
<input type="checkbox"/>	<u>5522054</u>	May 1996	Gunlock et al.	395/439
<input type="checkbox"/>	<u>5613074</u>	March 1997	Galloway	395/280
<input type="checkbox"/>	<u>5675723</u>	October 1997	Ekrot et al.	395/182.02
<input type="checkbox"/>	<u>5692200</u>	November 1997	Carlson et al.	395/735

☐ 5751977

May 1998

Alexander

395/306

ART-UNIT: 2181

PRIMARY-EXAMINER: Wong; Peter

ASSISTANT-EXAMINER: Glass; David S.

ATTY-AGENT-FIRM: Akin Gump Strauss Hauer &amp; Feld LLP

## ABSTRACT:

The present invention relates to a method of in-band communication, outside the standard SCSI communication protocol, between SCSI bus repeaters and initiator devices. The present invention implements the communication mode during the message phase of the SCSI protocol and allows initiators on a SCSI bus to determine the number, location and status of SCSI repeaters accessible on the SCSI bus.

33 Claims, 7 Drawing figures

First Hit   Fwd Refs

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L16: Entry 19 of 29

File: USPT

Nov 27, 1990

US-PAT-NO: 4974153

DOCUMENT-IDENTIFIER: US 4974153 A

TITLE: Repeater interlock scheme for transactions between two buses including transaction and interlock buffers

DATE-ISSUED: November 27, 1990

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Pimm; David W.	Nashua	NH		
Natusch; Paul J.	Westford	MA		
Silver; Robert T.	Marlboro	MA		

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Digital Equipment Corporation	Maynard	MA			02

APPL-NO: 07/ 162620   [PALM]

DATE FILED: March 1, 1988

## PARENT-CASE:

This is a continuation-in-part of application Ser. No. 093,501, filed Sept. 4, 1987, now U.S. Pat. No. 4,897,786.

INT-CL: [05] G06F 13/36, G06F 13/40

US-CL-ISSUED: 364/200; 340/825.5, 364/240.2, 364/239

US-CL-CURRENT: 710/306; 340/825.5

FIELD-OF-SEARCH: 364/2MSFile, 364/9MSFile, 340/825.5

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<u>4484267</u>	November 1984	Fletcher	364/200
<input type="checkbox"/>	<u>4604689</u>	August 1986	Burger	364/200

ART-UNIT: 238

PRIMARY-EXAMINER: Anderson; Lawrence E.

ATTY-AGENT-FIRM: Kenyon & Kenyon

ABSTRACT:

A system for implementing a repeater interlock scheme between a first and a second bus utilizes two repeaters. The first repeater coupled to the first bus includes an interlock state bit which is set upon the acceptance of an interlock transaction from a processor. No further interlock transactions will be accepted while the interlock state bit is set. The interlock transaction is passed to a transaction buffer in the second repeater which is coupled to memory through the second bus. The transaction buffer passes the interlock data for memory to the second bus while simultaneously loading a one deep interlock buffer. A confirmation is sent from the memory back to the transaction buffer. If the confirmation is interlock busy, then the interlock transaction is retried from the interlock buffer thus allowing the transaction buffer to process other commands. The interlock buffer waits for an unlock write signal before retrying an interlock transaction thus alleviating congestion on the second bus.

6 Claims, 16 Drawing figures